

EUV Lithography for 22nm Half Pitch and Beyond: Exploring Resolution, LWR, and Sensitivity Tradeoffs

Steve Putna, Todd Younkin, Roman Caudillo,
Terence Bacuita, Uday Shah, Michael Leeson,
Manish Chandhok

2010 International Symposium on EUV Lithography

Purpose of Work

- **Develop a Fundamental Mechanistic Understanding that Enables Realization of HVM Capable $\leq 22\text{nm}$ Half Pitch EUV Litho Materials**

Presentation Overview

- **Highlights**

- On track to evaluate ~500 materials by end of year
- MET C-Dipole illumination enables internal 22 hp BM
- Chemically Amplified Resist viable option for ≤ 30 HP

- **Lowlights**

- Resist only solution very challenging
- LWR, Collapse & 2D patterning need improvement

Intel MET

•EXPERIMENTAL :

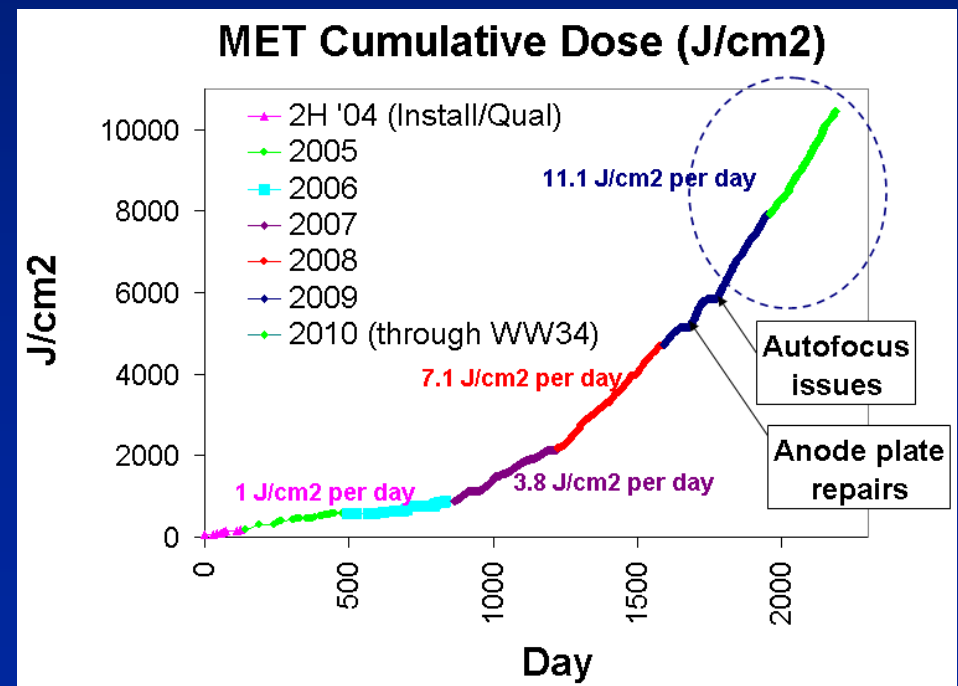
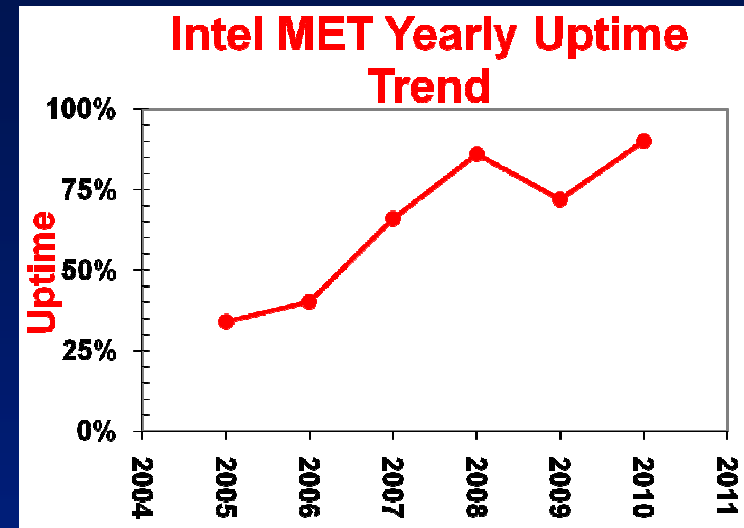
- $\lambda = 13.5$ nm, 0.3 NA
- Low Flare ~ 3 -6 %
- Field Size = 200 μ m x 600 μ m

•RELIABILITY :

- 90% uptime

•PRODUCTIVITY :

- Cumulative dose delivery \uparrow



Resist Screening Strategy, Protocols

- Intel MET = Primary development tool
 - SEMATECH MET = Secondary capability
- Focus on 1D L/S pattern
 - 1D L/S characterization = 30/26 hp PW + ≤ 24 hp UR
 - Depth of Focus typically limited by LWR
- 2D Patterning Benchmarks well against 1D Metrics
 - Validates 1D methodology / figures of merit
 - 2D metrics for champ materials assessed regularly

Material Focus Areas

[1] LWR

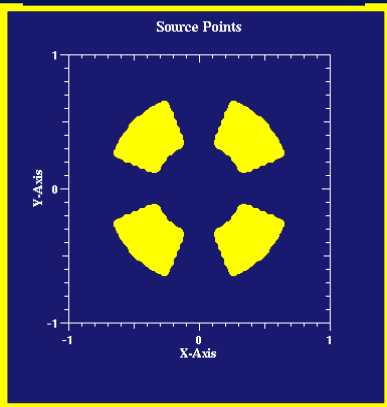
- Physical / chemical LWR reduction techniques
- Novel organic / inorganic ancillary materials
- External / Internal Post Processing Demo's
- Reduced LWR Reticles

[2] Pattern Collapse

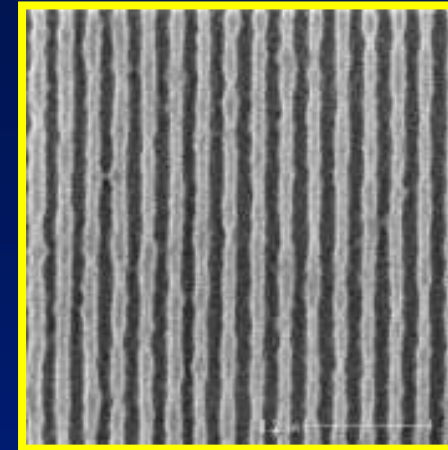
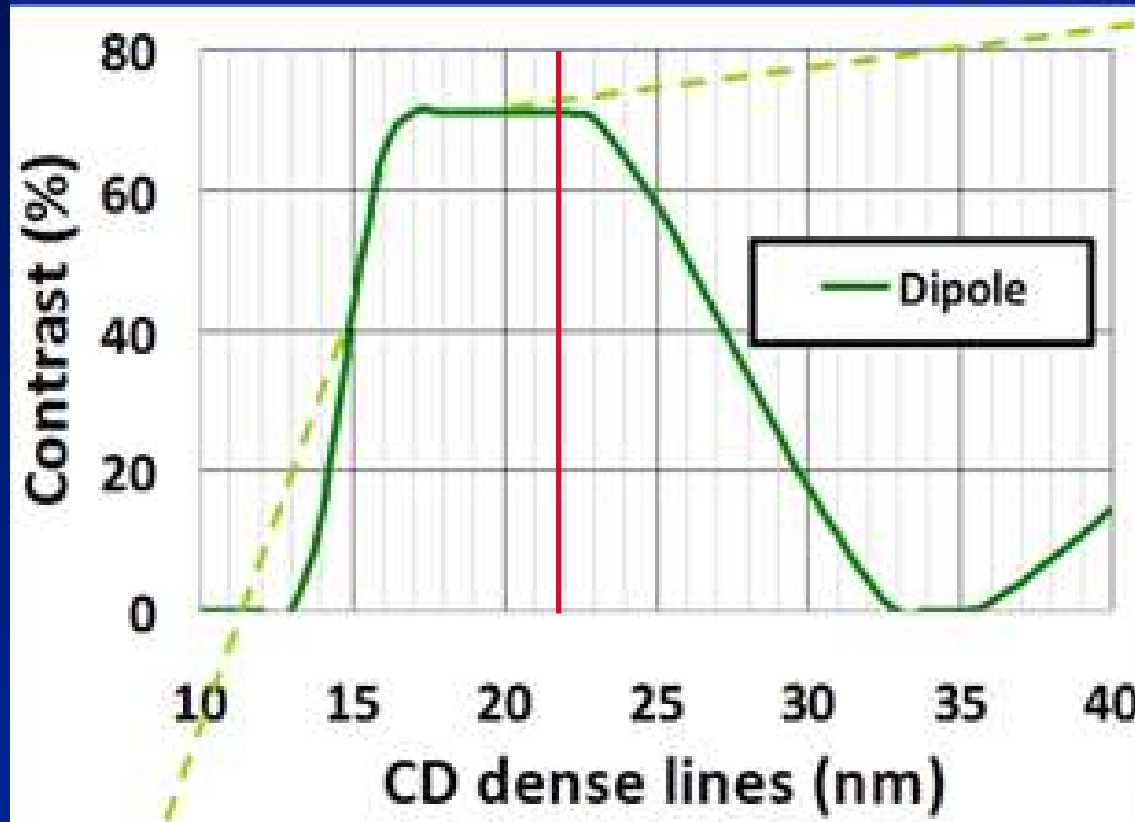
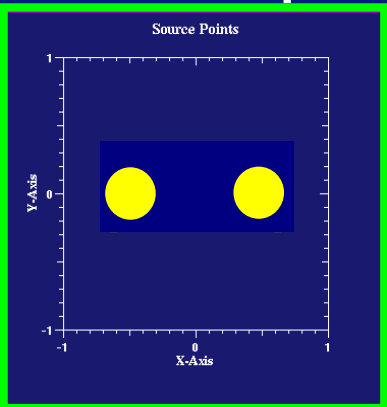
- Optimize Aspect Ratio / Surface Energy
- Increase Resist Modulus
- Reduce Developer / Rinse Surface Tension

Champion Resist Process + Dipole Illumination Enables 22nm HP Resolution

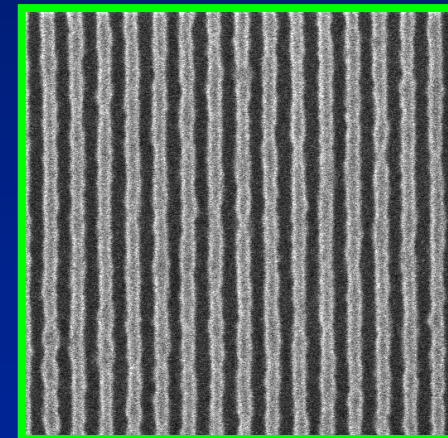
Quadrupole



On-axis dipole



22 nm HP



Minimum LWR = 4.3nm; Esize = 10.9mJ

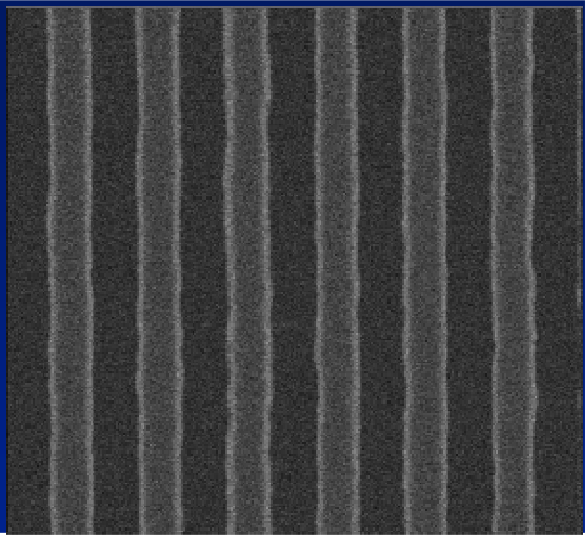
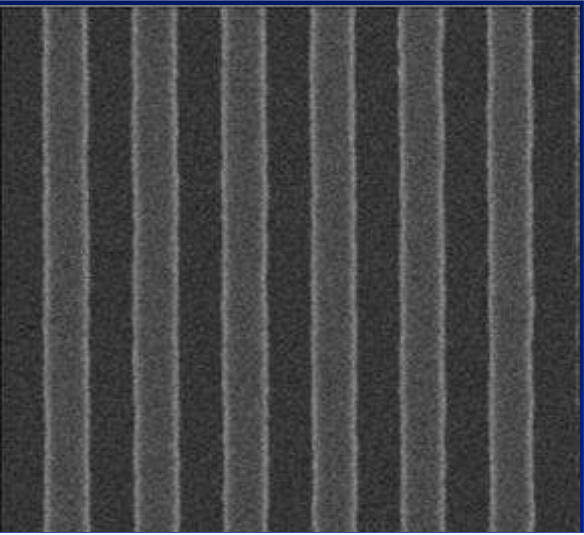
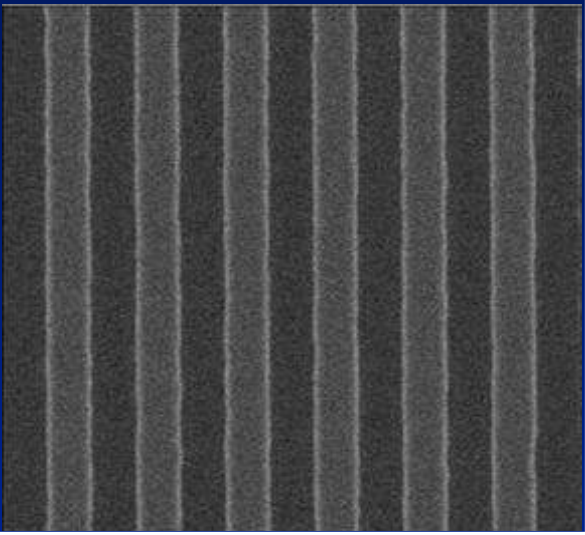
With 275nm DOF

Data Taken on Intel MET with NA = 0.30

LWR Reduction via Post Processing

- Strategies
 - Mask
 - Implant
 - Cure
 - Etch
 - Improved Tooling
 - Offsite Demonstrations
- Gap to Target / 2010 Goal
 - 22nm HP, **3.0nm LWR** @ 11.3mJ Esize

Mask LWR Reduction

Process A	Process B	Process C
		
LWR ~ 8.7	LWR ~ 4.7	LWR ~ 4.6

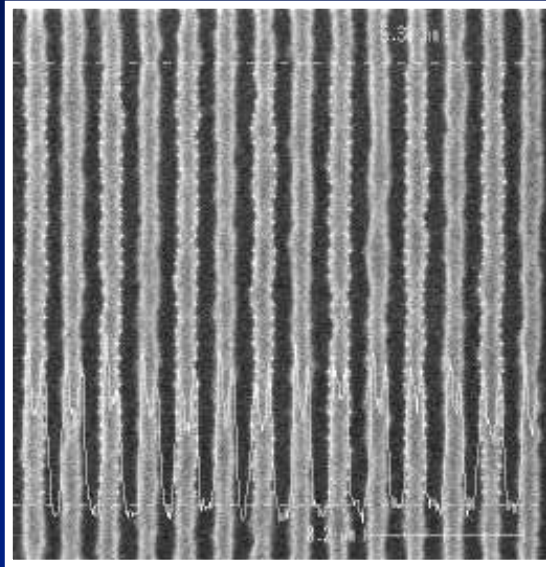
Improved process yields lower reticle LWR

Ion Implantation

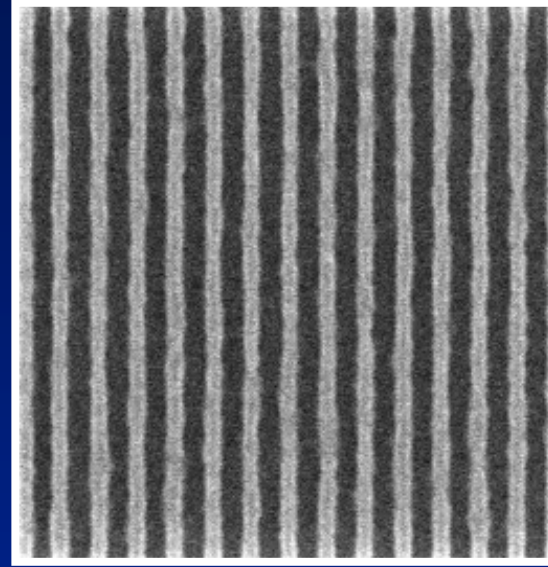
Implant Condition	% CD Change	% LWR Change
A	-11%	0%
B	-21%	0%
C	-11%	2%
D	-7%	2%
E	-10%	2%
F	-8%	10%
G	-16%	-3%
H	-18%	-15%
I	-11%	0%
J	-20%	-10%
K	-9%	-2%

Condition H provided highest 1D LWR reduction but CD shrinkage is observed

E-Beam Cure



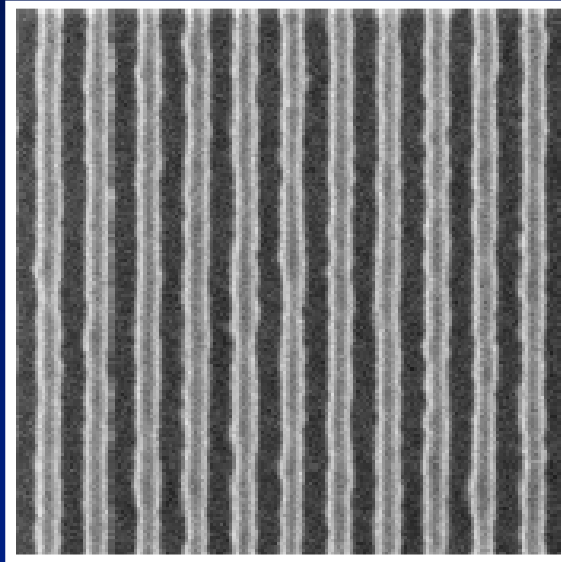
Pre



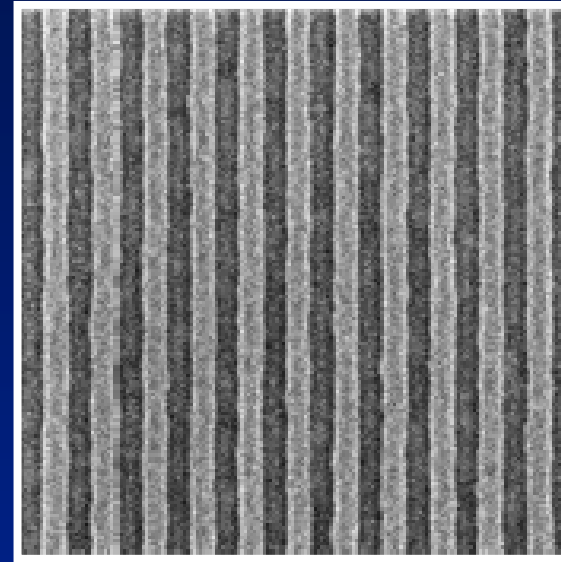
Post

EB Cure results in 20-25% CD + LWR Reduction

Bi-Layer Etch



Pre



Post

Etch results in 15-20% LWR reduction with no CD Bias

Observe LWR improvement in move from MET → IMEC ADT

	26 nm HP	28 nm HP	30 nm HP	40 nm HP	50 nm HP
Intel MET Esize ~ 14.5 mJ/cm ²					
LWR	6.9	4.8	4.9	4.6	4.1
IMEC ADT Esize ~ 13.0 mJ/cm ²					
LWR	5.9	4.6	3.6	3.1	2.4
	- 14 %	- 5 %	- 26 %	- 33 %	- 40 %

*Side-by-side comparison indicates
ADT can yield ~ 25% lower LWR than Intel MET*

Conclusions

- On track to evaluate ~ 500 materials prior to EOY
- Intel MET dipole illumination enables internal 22 hp BM
- PC and LWR need continued improvement
- 2D Patterning BMs well against 1D Figures of Merit
- <16 nm HP Aerial Image Capability Needed Soon

Intel EUVL Team

Todd Younkin (IMEC)
Terence Bacuita
James Blackwell (MAP)
Robert Bristol
Roman Caudillo
Manish Chandhok
Armando Cobarrubia
Kent Frasure
Long He
Ted Liang
Guojing Zhang

Michael Leeson
Yashesh Shroff
Alan Myers
Seh-jin Park
Bryan Rice (ISMT)
Jeanette Roberts
James Ryan
Gil Vandentop
Pei-Yang Yan
Edward Johnson
Wang Yueh